



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Warren M. Farnworth

Serial No.: 10/043,362

Filed: January 9, 2002

**For: STEREOLITHOGRAPHIC METHODS  
FOR FABRICATING HERMETIC  
SEMICONDUCTOR DEVICE PACKAGES  
AND SEMICONDUCTOR DEVICES  
INCLUDING  
STEREOLITHOGRAPHICALLY  
FABRICATED HERMETIC PACKAGES**

Examiner: Unknown

Group Art Unit: Unknown

Attorney Docket No.: 4212.1US (99-0306.1)

CERTIFICATE OF MAILING

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May 14, 2002  
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Deidra Pfeil  
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PRELIMINARY AMENDMENT

Box Non-Fee Amendment  
Commissioner for Patents  
Washington, D.C. 20231

Sir:

Prior to examination of the above-referenced patent application on the merits, entry of the amendments as set forth herein is respectfully solicited.

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#4 amendment into  
1/11/02  
5-29-02

IN THE CLAIMS:

Claim 16 has been amended herein. All of the pending claims 1 through 19 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Attached is a marked-up version of the claim amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

1. A packaged semiconductor device, comprising:  
a connection element;  
at least one semiconductor die operably connected to said connection element; and  
a hermetic package substantially sealing at least a portion of said at least one semiconductor die from an external environment, said hermetic package comprising a plurality of superimposed, contiguous, mutually adhered layers of a hermetic packaging material.
2. The packaged semiconductor device of claim 1, wherein said connection element comprises a carrier substrate.
3. The packaged semiconductor device of claim 2, wherein a surface of said at least one semiconductor die is disposed against said carrier substrate.
4. The packaged semiconductor device of claim 3, wherein said hermetic package covers at least another surface of said at least one semiconductor die.
5. The packaged semiconductor device of claim 1, wherein said connection element comprises a lead frame.
6. The packaged semiconductor device of claim 5, wherein said hermetic package covers at least said at least one semiconductor die.

7. The packaged semiconductor device of claim 6, wherein said hermetic package also covers a portion of said lead frame adjacent to said at least one semiconductor die.
8. The packaged semiconductor device of claim 1, wherein said hermetic packaging material comprises thermoplastic glass.
9. The packaged semiconductor device of claim 1, wherein said hermetic packaging material comprises ceramic or metal.
10. A substantially hermetically packaged semiconductor device, comprising:  
a semiconductor die; and  
a package surrounding at least a portion of said semiconductor die and substantially hermetically sealing same, said package comprising a plurality of superimposed, contiguous, mutually adhered layers, each of said layers comprising a thermoplastic glass.
11. The semiconductor device of claim 10, further comprising a carrier substrate connected to said semiconductor die.
12. The semiconductor device of claim 10, further comprising a lead frame connected to said semiconductor die and at least partially substantially hermetically sealed by said package.
13. The semiconductor device of claim 10, wherein said package further comprises at least one external circuit in communication with at least one bond pad of said semiconductor die.
14. A package for substantially hermetically packaging a semiconductor device, comprising at least one portion, said at least one portion comprising a plurality of superimposed, contiguous, mutually adhered layers of hermetic packaging material.

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15. The package of claim 14, wherein said at least one portion includes a receptacle configured to receive at least a portion of the semiconductor device and to substantially seal a semiconductor die of the semiconductor device from an environment external to the package.

16. (Amended) The package of claim 14, wherein the package further comprises another portion configured to be assembled with said at least one portion so as to substantially seal a semiconductor die of the semiconductor device from an environment external to the package.

17. The package of claim 16, wherein said another portion also comprises a plurality of superimposed, contiguous, mutually adhered layers of hermetic packaging material.

18. The package of claim 14, wherein said hermetic packaging material comprises a thermoplastic glass.

19. The package of claim 14, wherein said hermetic packaging material comprises a ceramic or a metal.

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**REMARKS**

No new matter has been added. The Applicant again requests entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Brick G. Power". The signature is fluid and cursive, with a long horizontal stroke extending to the right.

Brick G. Power  
Registration No. 38,581  
Attorney for Applicant  
TRASKBRITT  
P. O. Box 2550  
Salt Lake City, Utah 84110-2550  
Telephone: (801) 532-1922

Date: May 14, 2002

BGP/df